Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 12 (Cancelled)

13. (New) An information processing device comprising:

a DRAM having a burst mode which burst-transfers data of successive column addresses;

one or more data processing units operable to issue an access request; and

an address conversion unit operable to convert access addresses which are included in the access request issued from said one or more data processing units,

wherein at least one of said one or more data processing units is operable to access an M x N rectangular area, where M and N are integers,

said address conversion unit is operable to convert access addresses so that a column address of data at the (K+m)th column, where K and m are integers and $m \leqq M$, of an Lth line, and a column address of data at a Kth column of an (L+n)th line, where L and n are integers and $n \leqq N$, become successive, and

some or all areas of said DRAM is a frame memory which stores image data, the rectangular area is M pixels x N lines in the image data, and said data processing units are operable to perform one of motion compensation and motion estimation, where $n=2n'$ and n' is an integer.

14. (New) The information processing device according to Claim 13,

wherein another one of said data processing units is operable to access the image data on a line basis, and to continuously read out data of all 2n lines.

15. (New) The information processing device according to Claim 13,

wherein said data processing unit is operable to decode an inputted stream on a basis of two or more macroblocks, by motion compensation,

said DRAM is operable to store the image data decoded by said data processing unit,

said information processing device further comprises:

a memory featuring a smaller storage capacity and a faster access speed than said DRAM;

a data transfer unit operable to transfer the data from said DRAM to said memory, and

said data processing unit is operable to access the image data stored in said DRAM as reference data.

16. (New) The information processing device according to Claim 15,

wherein the image data stored in said DRAM is split into transfer regions larger in size than the rectangular area, and

said data transfer unit is operable to transfer data on a transfer region basis from said DRAM to said memory, based on the access request from said data processing unit.

17. (New) The information processing device according to Claim 15,

wherein said data transfer unit is operable to transfer a minimum area which surrounds plural rectangular areas as a transfer region as data from said DRAM to said memory, based on an access request from said data processing unit.

18. (New) The information processing device according to Claim 16,

wherein said data transfer unit includes a register which holds a size of the transfer region.

19. (New) The information processing device according to Claim 16,

wherein said data transfer unit is operable to transfer the data from said DRAM to said memory when a predetermined number n1 of access requests are outputted from said data processing unit.

20. (New) The information processing device according to Claim 19,

wherein said data transfer unit includes a register which holds the size of the transfer region and the number n1.

21. (New) The information processing device according to Claim 16,

wherein said data transfer unit is operable to transfer the transfer region which includes all rectangular areas, from said DRAM to said memory when access requests from said data processing unit request the rectangular areas which are adjacent or overlapping.

22. (New) The information processing device according to Claim 16, wherein said data processing unit includes:

a motion vector estimation unit operable to estimate plural motion vectors corresponding to plural macroblocks from the inputted stream; and

a decoding unit operable to decode the inputted stream on a macroblock basis, and to store a decoding result into said DRAM,

wherein a decoding sequence of the macroblocks is changed based on the plural motion vectors so that addresses for accessing said DRAM become successive.

23. (New) A data access method for accessing a rectangular area made up of M pixels x N lines in image data from a DRAM, the DRAM having a burst mode which burst-transfers data of continuous column addresses, and storing the image data, said data access method comprising:

an input step of inputting an access request for the rectangular area; and

an address converting step of converting access addresses included in an access request issued in said access step,

wherein in said address converting step, addresses are converted so that a column address of data at the (K+m)th column, where K and m are integers and $m \leqq M$, of the Lth line, and a column address of the data at the

Kth column of the (L+n) line, where L and n are integers and $n \leqq N$, become successive, and

some or all areas of said DRAM being a frame memory which stores image data and the rectangular area being M pixels x N lines in the image data, where M and N are integers, and a data processing unit performing motion compensation and motion estimation, where n=2n' (n' is an integer).

24. (New) The information processing device according to Claim 17,

wherein said data transfer unit is operable to transfer the data from said DRAM to said memory when a predetermined number n1 of access requests are outputted from said data processing unit.

25. (New) The information processing device according to Claim 24,

wherein said data transfer unit includes a register which holds the size of the transfer region and the number n1.

26. (New) The information processing device according to Claim 17,

wherein said data transfer unit is operable to transfer the transfer region which includes all rectangular areas, from said DRAM to said

memory when access requests from said data processing unit request the rectangular areas which are adjacent or overlapping.